ADQ214-DCLN Datasheet

ADQ214-DCLN is the solution for highly accurate low noise measurement situations. ADQ214-DCLN features:

- *2 analog channels sampling at 400 MSPS each for high bandwidth*
- *DC-coupled low noise front-end for high dynamic range*
- *Real-time decimation up to 2^{34} times for accurate analysis*
- *Open FPGA for real-time custom signal processing*
- *Data streaming for real time recording*

PXIe

USB2.0

SWEDEN | Signal Processing Devices Sweden AB | Teknikringen 6, SE-583 30 Linköping | Phone: +46 (0) 13 4650600 | Fax: +46 (0) 13 991 3044
SWITZERLAND | Signal Processing Devices | 275, Route de Saint-Julien, CH-1258 Perly, Geneva | Phone: +41 78 845 5657
US | Signal Processing Devices Inc. | 2603 Camino Ramon, Suite 200, San Ramon CA 94583 | Phone: +1 415 533 1341

www.spdevices.com

ADQ214-DCLN Datasheet

Features

- 2 analog channels
- 400 MSPS sample rate per channel
- 14 bits vertical resolution
- DC-coupled analog front-end
- 100 MHz analog BW
- Decimation up to 2^{34} times
- 32 bits output option for high SNR
- Internal and external clock reference
- Internal and external trigger
- Trigger output
- Time-stamp for real-time operation
- 64 MSamples/channel data memory
- Data interface PXIe / cPCIe / USB2.0

ADQ214 Development Kit

- FPGA open for custom applications
- Real-time signal processing

Applications

- Phase noise measurement
- Signal analysis
- Wireless communication
- Automated test
- Test and measurement
- Wideband IQ demodulator

Advantages

- Host PC form factor options for optimized system partitioning.
- Analog front-end optimized for low noise over a wide bandwidth.
- On-board decimation filter off-loads the CPU for optimized system design.
- Real-time custom data processing solutions for advanced systems.
- SP Devices' design service is available for fast integration to lower time-to-market.

1 Low noise data acquisition solution for measurement applications

1.1 ADQ214-DCLN design philosophy

The ADQ214-DCLN is designed particularly for measurement of low-level noise in the frequency range from very low frequencies, below 0.1 Hz, up to 100 MHz. This is enabled by the low noise DC-coupled front-end which has exemplary noise performance both in terms of 1/f-noise and wide-band noise, while also being very well shielded from external interference that could otherwise show up in the signal spectrum.

The front-end include 120 MHz analog low-pass filters that prevent energy from higher Nyquist bands (above 200 MHz) to appear at aliased frequencies in the digitized signals.

The low noise level of the DC-coupled front-end makes the ADQ214-DCLN an ideal fit for applications such as phase noise measurement systems, IQ-receivers, and high-resolution measurement of noise on power supplies and analog signals.

1.2 Decimation filter

After the signals have been digitized by the analog-to-digital converters, the ADQ214-DCLN can either store and transfer the data as is, i.e. as 14-bit values sampled at 400 MSPS, or the data rate can be reduced by a configurable number of steps of digital low-pass filtering and decimation. This decimation process effectively increases the resolution of the digitizer while reducing the sampling rate. This allows detailed study of lower frequency signals without the burden of having to deal with enormous amounts of data.

The programmable real-time decimation block can reduce the sampling rate by all powers of 2 between 2^3 and 2^{34}, resulting in decimated sampling frequencies of between 25 MHz and 0.023 Hz. Each step of the decimation process contains a low-pass filter that is close to ideal in terms of passband ripple and stop-band attenuation. The filters suppress the frequencies in the upper half of the Nyquist band and prevent aliasing from occurring when the data rate is decimated by a factor of 2 in each step.

The theory of decimation gives that each factor of 4 of decimation yields one extra bit of resolution, thus effectively increasing the dynamic range. To take full advantage of this fact, the ADQ214-DCLN stores and transfers decimated samples using 32 bits of resolution instead of the default 14 bits.

The decimation filter makes the ADQ214-DCLN very flexible and a wide variety of measurement needs can be fulfilled with the same device.

DECIMATION IP CONFIGURATIONS (EXAMPLES)			
Decimation	Sampling rate	Resolution	ENOB
$2^0 = 1$	400 MSPS	14 bits	10.5 bits
$2^4 = 16$	25 MSPS	16 bits	12.5 bits
$2^{12} = 4096$	98 kSPS	20 bits	16.5 bits

1.3 Idle channel noise level

Data collected at a variety of different decimation settings was used to efficiently create the plot in **Figure 1**, which demonstrates the idle channel noise performance from 0.1 Hz to 200 MHz, i.e. a frequency span of more than nine decades. The data batch size was kept the same while the sampling rate was varied through the use of decimation, resulting in different resolution bandwidths (RBW) in different parts of the spectrum.

The power of the built in decimation function is shown in the low frequency region of **Figure 1**. To get to an RBW of less than 0.1 Hz without the use of decimation would have required each batch of data to contain 4 Gsamples, which is more than the digitizer memory supports. It would also require an enormous amount of processing to calculate the FFTs and average the results.

1.4 Signal analysis applications

The very low noise level and the clean idle channel spectrum that is free from discrete noise tones give the ADQ214-DCLN a very large dynamic range, making it a particularly suitable tool for analyzing weak signals.

The ADQ214-DCLN is therefore ideal for phase noise measurement in lab environments as well as automated test equipment. The use is not limited to phase noise. Any wide band signal analysis, for example on power supply lines, benefits from the performance of ADQ214-DCLN.

1.5 IQ receiver application

Connecting the dual channels to an IQ demodulator and sampling the I and Q gives a high precision zero-IF receiver with up to 50 MHz bandwidth. The built-in decimation filter is ideal for reducing the data rate without losing signal quality. The data streaming feature enables real-time processing in a PC or recording to disk.

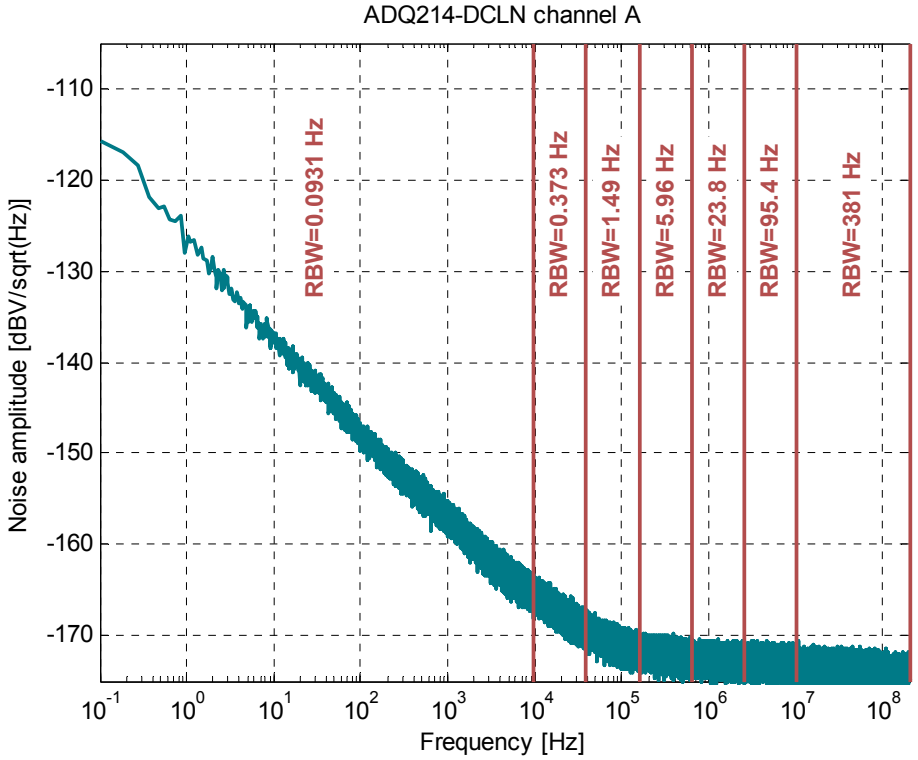


Figure 1: ADQ214-DCLN typical idle channel noise.

2 Technical data[1]

KEY PARAMETERS		
Number of channels		2
Vertical resolution	[bits]	14
Noise level @ 1MHz	[nV / √Hz]	3.1
Sampling rate / channel	[MSPS]	70 - 400
Data memory	[MBytes]	256
Trigger		Software / External / Level
Clock source		Internal / External / Ext. reference

ANALOG INPUT		
ENOB @ 1-70 MHz	[bits]	10.5
SFDR @ 1 MHz	[dB]	80
SFDR @ 40 MHz	[dB]	76
Impedance DC	[Ω]	50
Bandwidth (–3 dB)	[MHz]	DC – 120
Bandwidth (–1 dB)	[MHz]	DC – 100
Input voltage range	[mV_{pp}]	650
Noise level @ 10 Hz	[dBV/√Hz]	-137
Noise level @ 100 kHz	[dBV/√Hz]	-170
Connector		SMA

TRIGGER INPUT/OUTPUT		
External trigger input		
Input impedance DC	[Ω]	50
Input range (min – max)	[V]	–2.5 – +3.3
Threshold rising edge	[V]	0.5
Time resolution	[ps]	625
External trigger output		
Output impedance	[Ω]	20
Output (low – high)	[V]	0.1 – 2 (no load)
Trigger control		
Pre-trigger buffer		Up to batch size
Trigger hold off	[samples]	2^{33}
Pulse repetition frequency	[MHz]	1.6
Connector		SMA

CLOCK		
Internal TCXO Clock Reference		
Frequency	[MHz]	10
Accuracy	[ppm]	± 5 ± 0.5/year
Jitter RMS	[fs]	400
External Clock Reference		
Frequency	[MHz]	1 – 200
Signal level (min – max)	[Vpp]	0.8 – 3.3
Impedance AC	[Ω]	50
Added Jitter RMS	[fs]	400
Internal Clock		
Sample rate nominal	[MHz]	400
Sample rate settings	[MHz]	800/n, n=2...11
Reference sources		Internal TCXO External
External Clock		
Frequency (min – max)	[MHz]	70 - 400
Signal level (min – max)	[V_{pp}]	0.25 – 2
Impedance AC	[Ω]	50
Duty cycle	[%]	50 ± 5
Connector		SMA
Clock frequency control		
Sample skip factor		2 X n up to 2^{17} (n is an integer)
Decimation factor		2^{d} (d is 3 to 34)

GPIO		
Number of bi-directional signals		5
Output imp. GPIO-pin 5	[Ω]	30
Output imp. GPIO-pin 1–4	[Ω]	100
Output low max	[V]	0.1 (no load)
Output high min	[V]	3.1 (no load)
Input impedance	[kΩ]	10
Input low max	[V]	0.8
Input high min	[V]	2.3
Connector		Micro-D plug 9 w

1. All values are typical unless otherwise noted.

HOST PC INTERFACE		
USB2.0 (option –USB)		
Sustained data rate	[MBytes/s]	25
Connector		Mini–B
PXI Express (option –PXIE)		
Sustained data rate	[MBytes/s]	790
Lane bit rate		Generation 1
Lanes		4

ENVIRONMENTAL / MECHANICAL		
Operating temperature	[^{o}C]	0 – 45
Storage temperature	[^{o}C]	–20 – 70
Case size (–USB)	[mm^3]	103 x 166 x 31
Size (–PXIE)		1 slot 3U 4TE
Supply voltage	[V]	12
Power consumption	[W]	26
Certification and compliance		CE, RoHS2

OPERATING SYSTEM	
Operating system	
Windows 7	32-bit and 64-bit
Windows 8 / 8.1	32-bit and 64-bit
Windows 10	When available
Linux[1]	Main distributions
Application software	
ADCaptureLab[2]	Acquisition and analysis
MATLAB[2]	API, examples
C/C++	API, examples
.Net (C#, Visual Basic)	API, examples
Python	Example scripts
LabVIEW	DLL import

1. Contact SP Devices sales representative for information about distributions.
2. Windows only.

3 Absolute Maximum ratings

Exposure to conditions exceeding these rating may reduce life time or permanently damage the device.

ABSOLUTE MAXIMUM RATINGS	Min	Max
Supply voltage (to GND)	–0.4 V	14 V
Analog input (AC)		4 V_{PP}
Analog input (DC)	–1.4 V	1.4 V
Trigger input (to GND)	–3 V	3.7 V
Clock input (AC)		3.3 V_{PP}
GPIO input (to GND)[1]	–1 V	4.6 V
Ambient temperature (operation)	0 ^{o}C	45 ^{o}C

1. A voltage on a GPIO input higher than 3.3 V may change the output voltage on GPIOs which are set to outputs. This may damage external equipment.

The ADQ214-DCLN USB version has a built-in fan to cool the device. If the air flow is blocked or the fan malfunctions, the temperature monitoring unit will protect the device from overheating by shutting down parts of the device.

The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

4 Performance plots

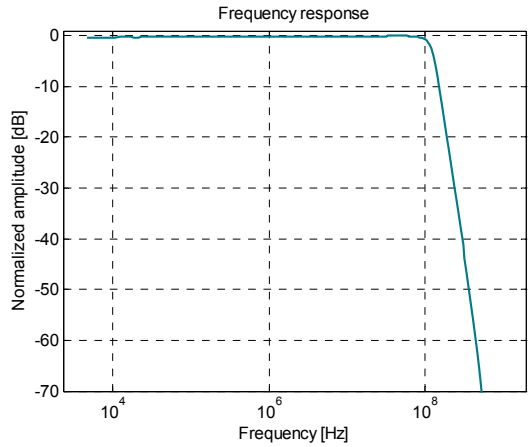


Figure 2: Frequency response.

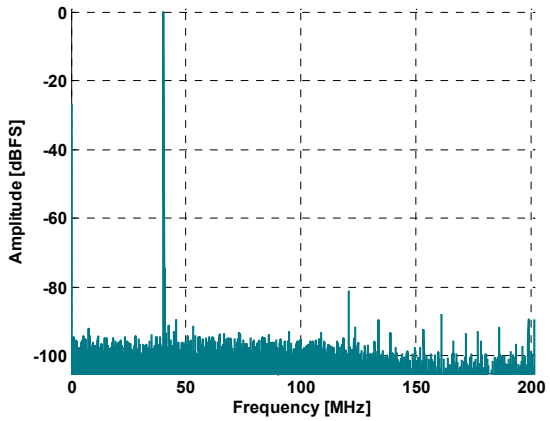


Figure 3: Frequency domain 40 MHz @ –1dBFS.

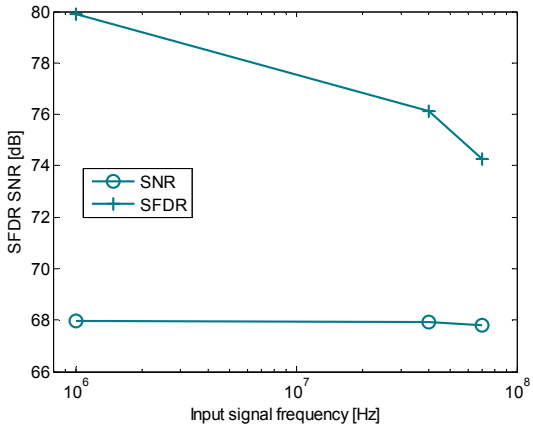


Figure 4: Input signal frequency sweep

5 Functional overview

5.1 Architecture

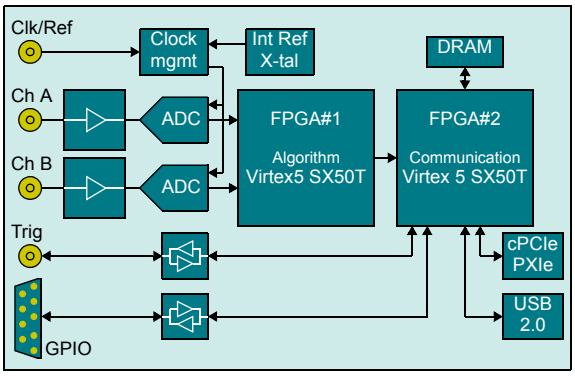


Figure 5: Block diagram

5.2 Analog front-end, AFE

The analog input is a DC-coupled single-ended input with 50 Ohm termination. The AFE also contains a 120 MHz low-pass filter to limit noise and aliasing.

The ADCs are 14-bit 400 MSPS high precision ADCs.

5.3 Clock

There are several modes for clocking the digitizer:

Internal clock for stand-alone operation.

External clock reference input for synchronization to external equipment.

External clock input for synchronization to external equipment.

5.4 Setting the sample rate

There are several ways of setting the sample rate.

- Setting the frequency in the PLL by adjusting the dividers.
- Applying an external clock.
- Applying an external reference. This is especially useful for locking several ADQ214-DCLN to the same frequency.
- Using the sample skip function. The ADCs operate at full rate while only a fraction of the samples are kept. In this way a large number of different sampling rates can be achieved and long measurement times are enabled.
- Using the decimation filter function. This is similar to the sample skip function, but with anti-aliasing filters for noise reduction and

aliasing prevention between each stage of sample rate reduction.

5.5 FPGAs

The ADQ214-DCLN is equipped with two powerful Xilinx XC5VSX50T-1 FPGAs. The FPGAs are partly open for custom real-time signal processing through the ADQ214 Development Kit.

The ADQ214 Development Kit is a tool that opens up the FPGA for custom real-time implementations. The ADQ214 Development Kit is purchased separately.

5.6 Trigger

The ADQ214-DCLN has several trigger options, which are summarized below.

Software trigger, where data capture is triggered by a software command. This is suitable for measurements on continuous waves.

Level trigger, where data capture is triggered by an event on the input data.

External trigger, where data capture is triggered by the edge on the trigger input connector. This is intended for synchronizing the signal source with the ADQ214-DCLN. It can also be used for synchronizing multiple ADQ214-DCLN units.

Internal trigger, where an internal timer generates triggers.

Pre-trigger buffer and trigger hold-off are available for control of the trigger position relative to the acquired data record.

5.7 Time-stamp

A 64-bit time counter, which runs at the sampling frequency, enables a time stamp for each event. At each trigger event, the counter value is stored together with the data record.

5.8 Data recording

There are several methods for data recording to serve different use cases:

Multi-record recording in on-board DRAM for very long records. There is 64 MSamples data memory per channel.

Continuous streaming of data to the host PC for real-time analysis of data.[1]

1. This mode requires data rate reduction, for example, decimation, sample skip, or custom implementation using the ADQ214 Development Kit.

5.9 Signal processing

There is support for real-time signal processing on the digitizer:

Level trigger for event detection.

Gain and offset digital tuning for range adjustment.

Decimation filtering for low noise measurements.

Custom real-time signal processing can be implemented in the FPGA using the ADQ214 Development Kit.

5.10 GPIO

The ADQ214-DCLN is equipped with five bi-directional GPIOs with short circuit protection, **Figure 6**. The GPIOs are individually controlled from software, but can also be accessed from the ADQ214 Development Kit.

The connector is a Micro D plug 9 way. A suitable socket cable is MOLEX 83421-9044.

#	Function
1	GPIO
2	GPIO
3	GPIO
4	GPIO
5	GPIO
6	GND
7	GND
8	GND
9	GND

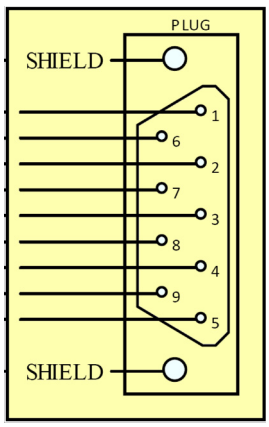


Figure 6: GPIO connections.

6 Software

6.1 Operating systems

The software package includes drivers for Windows and Linux operating systems.

6.2 Software development kit (SDK)

The ADQ214-DCLN digitizer is easily integrated into the application by using the software development kit. The SDK is included with the ADQ214-DCLN.

The SDK includes programming examples and reference projects. The ADQAPI user's guide describes all functions in detail. Many examples

and application notes simplify the integration process.

Using the SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

6.3 ADCaptureLab stand alone application

The ADQ214-DCLN is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time-domain and frequency-domain analysis, see **Figure 7**. Data can be saved in different file formats for off-line analysis. With ADCaptureLab, the ADQ214-DCLN operates as a desktop oscilloscope.

ADCaptureLab is available for Windows only.

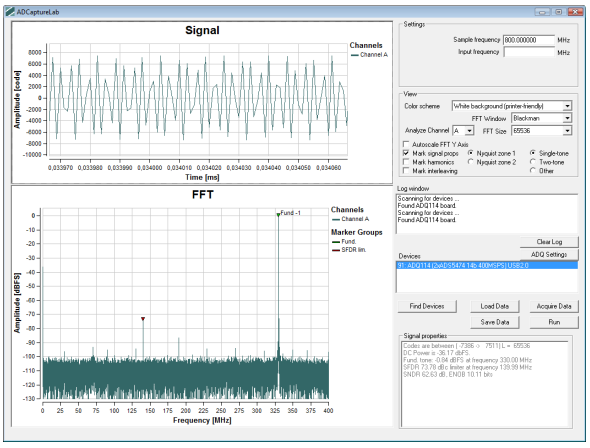


Figure 7: ADCaptureLab (Typical).

7 Host interface options

7.1 Stand-alone operation with USB2.0 interface (–USB)

The High Speed USB (USB 2.0) interface is intended for stand-alone operation and allows the ADQ214-DCLN to be integrated with the sensor system rather than the host PC.

With the USB2.0 interface, the digitizer is easily connected to any computer. The sustained data rate can be up to 25 MBytes/s and combined with on-board signal processing, an efficient solution is available. This is a suitable format for lab equipment.

The USB version is powered from an external power supply adapter. Use only the supplied adapter.

Figure 8: ADQ214-DCLN-USB.

7.2 Modular instrumentation with cPCIe / PXIe (–PXIE)

The cPCIe /PXIe form factor is intended for integration into a chassis for modular instrumentation. This is a preferred format in automated test equipment.

The ADQ214-DCLN can operate in either Compact PCI Express or PXI Express chassis.

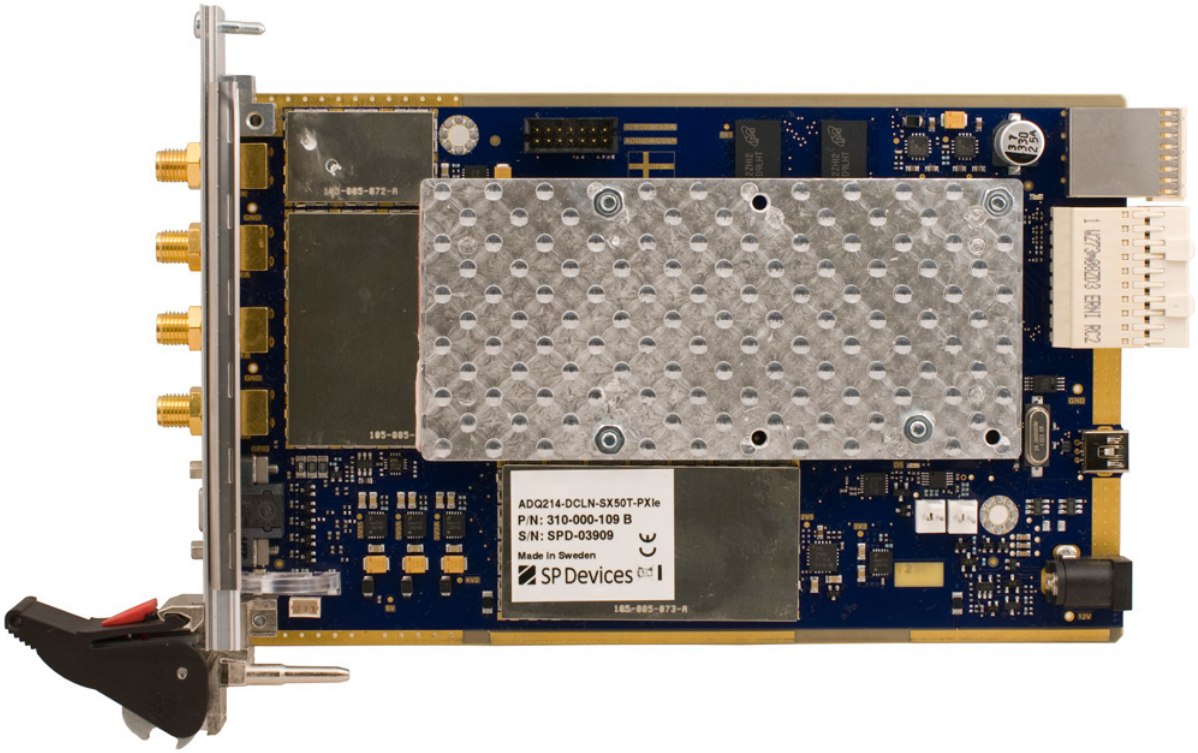
The PXIe card is powered from the chassis 12 V supply rail.

Figure 9: ADQ214-DCLN-PXIe.

Ordering information

ORDERING INFORMATION	
ADQ214-DCLN	ADQ214-DCLN
AVAILABLE OPTIONS	
Host PC interface USB2.0	–USB
Host PC interface PXI Express	–PXIE
RELATED PRODUCTS	
ADQ214 Development Kit	ADQ214 Development Kit

Example: ADQ214-DCLN-PXIE



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www.spdevices.com

SP Devices Corporate Headquarters

Teknikringen 6
SE-583 30 Linköping
Sweden

Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com